Springer

Journal of Mechanical Science and Technology 22 (2008) 1483~1489

Journal of Mechanical Science and Technology

www.springerlink.com/content/1738-494x
DOI 10.1007/s12206-008-0502-x

A study on the thermomechanical behavior of semiconductor chips on thin silicon substrate

Jae Hyuk Lim[1], ManHee Han[2], Jun-Youn Lee[3], Youn Young Earmme[3], Soon-bok Lee[3] and Seyoung Im[3,*]

[1]*Satellite Structure Department, Satellite Technology Development Office, Korea Aerospace Research Institute (KARI), 115 Gwahangno 45 Eoeun-dong Yuseong-gu, Daejeon 305-333, Korea*
[2]*Device Package Center, Semiconductor Buisiness, Samsung Electronics CO. LTD., #723 Buksu-Ri, Baebang-Myeon, Ansan-City, Chungcheongnam-Do 336-711, Korea*
[3]*Department of Mechanical Engineering, Korea Advanced Institute of Science and Technology (KAIST), Science Town, Daejeon 305-701, Korea*

(Manuscript Received December 31, 2007; Revised April 21, 2008; Accepted May 4, 2008)

Abstract

This study is concerned with the deformation or warping behavior of thin layered semiconductor structure comprising a silicon substrate, a pattern layer and a polyimide coating layer with its thickness varying from 100um to 50 um. In contrast with the conventional thick semiconductor structure, today's semiconductor structure is increasingly thin and therefore the warping is extremely conspicuous, being among the major concerns in the structural design of a chip. In the view of thermomechanical analysis of an extremely thin layer structure considered in the present paper, a few parameters on the deformation should be taken into consideration such as the pattern layer and intrinsic stress. To account for the effect of the pattern layer, we make a well educated guess for the mechanical properties, employing the test results and the CBA (Composite Beam Analysis) theory. In addition, we take into consideration the effect of the intrinsic stress due to moisture absorption on deformation. We show that the chip warpage is accurately predicted when all these are properly considered. Furthermore, we have found that the local instability or wrinkling, associated with the nonuniformity or the inhomogeneity in material properties and bonding quality between any two neighboring layers, appears as one important mode of energy relaxation in addition to the overall warpage when the chip thickness becomes very small.

Keywords: Pattern layer; Thin silicon substrate; Thermomechanical analysis; Wrinkling

1. Introduction

Memory package products are becoming increasingly thinner and multi-functional for the application of mobile microelectronics. Stacking techniques of multiple semiconductor chips inside a thin package are now among the essential parts of today's advanced packaging technologies. For stacking a greater number of chips, the chip thickness has to be thinner, but this induces adverse effects on the stiffness or the strength of the chip. As the chip thickness is decreased, chip deformation is severer, causing a nonbonded area between the chip bottom and the PCB (Printed Circuit Board) substrate during die attach process, and chip delamination as well after the molding process. This leads to a drastically increasing possibility of memory breakdown.

Warpage δ is a measure of the deformation resulting from CTE (Coefficient of Thermal Expansion) mismatch between different layers of a multiple layered structure as seen in Fig. 1. The CTE mismatch stress remains in the wafer during the fabrication, thus causing chip warpage when chips are thinned through

*Corresponding author. Tel.: +82 42 869 3028, Fax.: +82 42 869 3210
E-mail address: sim@kaist.ac.kr
© KSME & Springer 2008

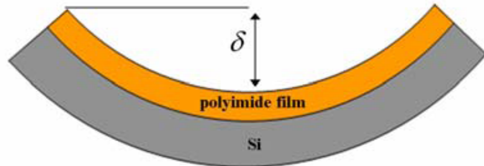

Fig. 1. Configuration of the out-of-plane deformation of the chip due to CTE mismatch.

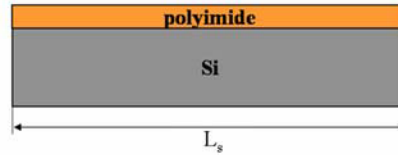

Fig. 2. Schematic view of polyimide on the Si substrate at the stress-free state.

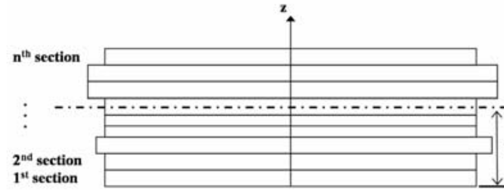

Fig. 3. Schematic view of multi-layered structure.

wafer back-grinding process. To predict the warpage and residual stress, several analytical methods have been proposed [1-6]. However, most of them are inappropriate for analyzing thin silicon chips in that the substrate is much thicker than polyimide film in these methods: the thickness ratio of polyimide film versus substrate should be less than 1/20 [1-3] although more enhanced methods have been proposed to cover the higher thickness ratios approximately [4-6]. In the present study, we employ finite element method (commercial software ABAQUS [7]) to predict the deformation behavior of thin silicon semiconductor chips.

In addition, there are a few unknown parameters that should be clarified such as material properties of the pattern layer, and stress-free temperatures of materials. The integrated circuit pattern structure on silicon wafer is fabricated through many unit processes such as diffusion, oxidation, metallization, etching and passivation on a silicon wafer, thus naturally consisting of complex and tiny materials. It would be impossible to model the pattern structure considering every tiny and complex component in detail. Therefore, we extract its equivalent material properties by fitting the test results to the CBA (Composite Beam Analysis) together with homogeneity assumption.

The outline of the paper is as follows. We provide a brief review of composite beam analysis and experimental arrangement of semiconductor chips in Section 2, and this is followed by the prediction of uncertain material properties in Section 3 and 4. In Section 5, we compare the analysis result with the test result to demonstrate the performance of the proposed study. Finally, we end with some concluding remarks.

2. Composite beam analysis and experimental arrangement of semiconductor chips

Consider a two-layered beam structure of polyimide coating on silicon substrate as depicted in Fig. 2. The two layers are in a state of zero stress at stress-free temperature of polyimide coating. Cooled to room temperature, the polyimide coating and silicon substrate have different thermal expansion due to the difference in CTE between the two materials when they are not boned. To make the deformations of two layers matched, a certain amount of stress needs to be imposed on the polyimide coating. Such sort of stress is defined to be the equivalent stress ($=\sigma_T$) in the axial direction as below

$$\sigma_T = E_f(\alpha_f - \alpha_s)(T_f - T_a) \tag{1}$$

where E, α is Young's modulus and CTE, respectively, and the subscripts "f" and "s" indicate polyimide film and silicon substrate; T_f and T_a are the stress-free temperature of the film and the ambient temperature, respectively. The effective radius of the deformed beam R, effective bending moment $M_{effective}$, flexural rigidity $EI_{effective}$ and distance η from the bottom to the neutral axis of the multi-layered beam structure as seen in Fig. 3 are expressed as follows [8]:

$$\frac{1}{R} = \frac{M_{effective}}{(EI)_{effective}} = \frac{12\sum_{i=1}^{n} E_i t_i w_i (\eta_i - \eta)(\alpha_i - \alpha_s)(T_{f,i} - T_a)}{\sum_{j=1}^{n} E_j t_j w_j \left[t_j^2 + 12(\eta_j - \eta)^2 \right]} \tag{2}$$

where

$$\eta_i = \sum_{k=1}^{i} t_k - t_i/2, \quad \eta = \left(\sum_{i=1}^{n} E_i w_i t_i \eta_i \right) \Big/ \left(\sum_{i=1}^{n} E_i w_i t_i \right),$$

$$(EI)_{effective} = \sum_{i=1}^{n} E_i w_i t_i \left[\frac{t_i^2}{12} + (\eta_i - \eta)^2 \right]$$

$$M_{effective} = \sum_{i=1}^{n} E_i w_i t_i (\eta_i - \eta)(\alpha_i - \alpha_s)(T_i - T_a) = \sum_{i=1}^{n} \sigma_T(i) w_i t_i (\eta_i - \eta)$$

Finally we obtain the warpage value δ from the following Eq. (3) [1-6].

$$\delta = \frac{L_s^{\,2}}{8R} \qquad (3)$$

Where L_s is the chip size in the longitudinal direction (see Fig. 2). To apply the multi-layered beam theory for laminated plates under thermal deformation, we replace E with the biaxial modulus $\tilde{E}$ while the isotropy of the biaxial modulus is preserved, where $\tilde{E}$ is defined as $\tilde{E} = E/(1-\nu)$ for isotropic material, $\tilde{E} = (C_{11}^2 + C_{11}C_{12} - 2C_{12}^2)/C_{11}$ for cubic material such as a (100) silicon wafer. Note that the use of the beam theory for plates is valid only for isotropic plates or for plates made of cubic materials with (100) or (111) orientation [9].

From Eq. (3), warpage is a function of the material properties of individual layers such as polymer coating, pattern and silicon substrate. The material properties of polymer and silicon are given in Table 1. However, the material properties of the pattern layer are still unknown because we have only little information on their material components and its detailed structure, although a few major components of pattern have become well-known such as silicon oxide, metal and so forth. We may be allowed to neglect the effect of the pattern layer on the overall deformation behavior of the chip for conventional thick chip structure [1-6]. However, for today's increasingly thin chip structures, the pattern layer occupies a substantial part of the chip cross-section, and it is imperative to account for the stiffness and other material properties of the pattern layer for accurate evaluation of the chip warpage. This may be verified through observation of the warpage of a thin chip which is composed of the silicon and the pattern layer with its top polyimide layer having been removed as shown in Table 2 and Fig. 11 (c) and 11 (d). The conventional thick chip structure hardly undergoes a warpage when its polyimide layer is stripped off. To take into consideration the presence of the pattern layer, we extract some equivalent material properties for the pattern layer,

Table 1. Material properties of single chip device.

Materials	E (Gpa)	Poisson's ratio	α (10^{-6}/°C)
polyimide (pix-3400)	3.0	0.34	46
pattern	-	-	-
silicon	C_{11}=165.7Gpa, C_{12}=63.9Gpa, C_{44}=79.6 Gpa		3.084+0.00196T (°C)
	t (μm)		Curing Temperature (°C)
polyimide (pix-3400)	10.0		329
pattern	4.5		-
silicon	35.5~85.5		

'-' Indicate unknown variable

Table 2. Measurement of warpage after drying.

Structure	Thickness (μm)	Warpage (μm)			Increment percentage (%)
		Prior to drying	30 min 250°C	30 min 300°C	
polyimide/ pattern/Si	100	20.8	25.5	27.6	32.7
	80	34.4	41.8	42.3	23.0
	60	56.0	69.3	70.1	25.2
	50	63.5	76.6	75.2	18.4
pattern/Si	70	15.6	16.8	16.5	5.8

under the assumption of isotropy and homogeneity of material, by fitting test results to CBA theory. For the measurement of chip warpage and deformation profile, a Twyman-Green interferometer [10-11] is used. To measure chip warpage according to temperature, we chose the following two types of chip samples: intact original samples of which the cross-sectional layout is polyimide/ pattern/silicon substrate with the total thicknesses of 50, 60, 80 and 100 μm as depicted in Fig. 4 (a), and polyimide-removed samples of which the layout is pattern/silicon substrate with thicknesses of 50, 70 and 90 μm as depicted in Fig. 4 (b). The planar chip dimension is 8850 μm by 4400 μm for both of the samples. The thickness of the polyimide coating layer and the pattern layer is fixed as 10 μm and 4.5 μm, respectively for all the samples as depicted Fig. 5.

The intrinsic stress due to water absorption has a significant effect on the chip warpage, particularly being prominent for thin chip structures [4-6]. Therefore, we have put all of the chip samples in a heat chamber at 250°C and 300°C for 30minutes, respectively, to remove the intrinsic stress effect due to moisture absorption. The test results for chips with

different thicknesses regarding this effect are summarized in Table 2. It is noted that the magnitude of chip warpage increased up to about 20 - 30% after drying for the first type samples, which retained the polyimide layer.

3. Prediction of material properties of the pattern layer

The pattern layer, which is made of various materials such as silicon nitride (SiN), aluminum (Al), and oxides, consists of several tiny and complex structures including metal lines, metal pads, vias, interlayer dielectric (ILD), shallow trench isolation, barrier metals and inorganic passivation layers. This kind of multiscale structure would not be tractable to a strict computational modeling as it is, i.e., it is too complex to model the entire structure in detail. Accordingly, we assume that this layer is comprised of a single homogeneous material and find the equivalent material properties. The equivalent material properties of the pattern layer are then calculated by fitting measured warpage results to CBA analysis as follows.

Consider here two beams as depicted in Fig. 4 (a) and 4 (b). One has the original cross sectional layout of polyimide/ pattern/ Si substrate, and the other the layout of pattern/ Si substrate with the polyimide layer being removed. Warpage of each beam structure is denoted as δ_1 and δ_2 for Fig. 4 (a) and for Fig. 4 (b), respectively, in the following Eqs. (4)-(5) from CBA theory with the modulus having been adjusted for the application to plates,

$$\delta_1 = \frac{M_{Effective} L_s^2}{8(\tilde{E}I)_{Effective}} \quad \text{(polyimide/pattern/Si)} \tag{4}$$

$$\delta_2 = \frac{M_{Effective} L_s^2}{8(\tilde{E}I)_{Effective}} \quad \text{(pattern/Si)} \tag{5}$$

Where δ_1 and δ_2 are obtained through the test results for 100 μm (polyimide/pattern/Si), and 90 μm (polyimide/pattern) specimens. Young's modulus, Poisson's ratio and CTE of the pattern layer can be obtained after solving Eqs. (4) - (5), iteratively as they have two unknown variables, $\tilde{E}$ and α. This procedure yields $\tilde{E}$ =300GPa and α =4.0 × 10^{-6}/°C. Then, the equivalent Young's modulus of the pattern layer is obtained as 210 GPa under the assumption ν =0.3 as summarized in Table 3. This assumption hardly affects the warpage, as long as $\tilde{E}$ remains invariant, from the view of CBA, which expresses the warpage in terms of $\tilde{E}$ and α.

Table 3. Material properties of pattern layer.

material	$\tilde{E}$ (Gpa)	E (Gpa)	Poisson's ratio	α (10^{-6}/°C)
pattern	300	210	0.3 (=assumption)	4.0

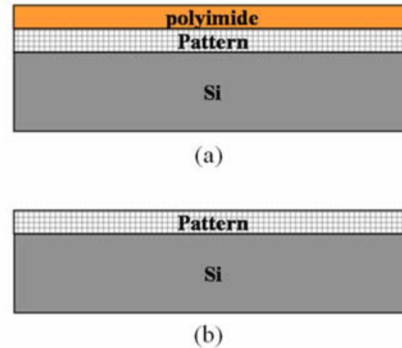

Fig. 4. Schematic view of a single chip: (a) polyimide coating/ pattern/ Si (b) pattern/Si.

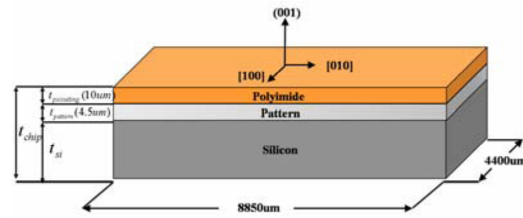

Fig. 5. Geometry and dimension of a single chip.

4. Prediction of the stress-free temperature of pattern and polymer coating

A composite beam-like structure covered with thin films has residual stress at room temperature due to CTE mismatch, thus being deformed severely when the thickness of beam is thin. By increasing temperature, it turns to stress-free state with negligible deformation at a critical temperature. It is the stress-free temperature of material which makes interaction to be insignificant with substrate. To obtain the stress-free temperature of the pattern layer, we measure the warpage in the range from room temperature 25°C to 340°C, which is the maximum limit temperature of the test device. The stress-free temperatures of both pattern layer and polyimide coating layer were determined by taking the linear regression on the measured warpage versus temperature. To determine the stress-free temperature of the pattern and the polyimide layer, we used two kinds of specimens: one consisting

of pattern/Si with total thickness 100 μm and 60 μm, and the other consisting of polyimide/pattern/Si with total thickness 100 μm and 80 μm. The warpage of specimens comprised of pattern/Si decreases almost linearly as temperature is increased, and will go to zero value around 400°C as seen in Fig. 6. Polyimide/pattern/Si specimen, however, shows a variation of slope according to temperature change as seen in Fig. 7. The reason for this is that the polyimide layer becomes inactive over its stress-free temperature. Finally, we obtain the stress-free temperature of the polyimide coating layer and the pattern layer as 280°C and 400°C in Table 4, respectively. To observe the warpage according to temperature, we have utilized the Twymann-Green interferometer [10-11]. Fig. 8 shows the fringes representing the warpage at different temperatures: 94 °C in Fig. 8 (a), 202 °C in Fig. 8 (b) and 336 °C in Fig. 8 (c). Note that the number of the fringes decreases as temperature goes up.

Table 4. Stress-free temperatures of pattern and polyimide coating.

material	Stress-free temperature (°C)
pattern	400
Polyimide (pix-3400)	280

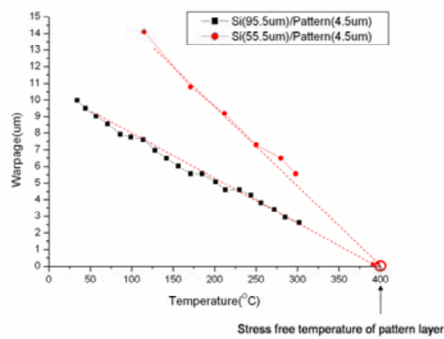

Fig. 6. Stress-free temperature estimation of the pattern layer using linear regression.

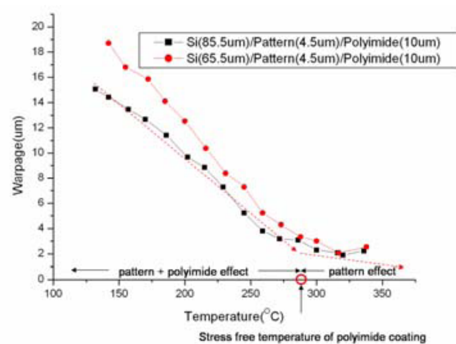

Fig. 7. Stress-free temperature estimation of the polyimide coating using linear regression.

5. Thermomechanical analysis

The warpage results for both test and finite element simulation through ABAQUS [7] are plotted versus the total chip thickness in Fig. 9. We model a quarter of the chip by imposing proper symmetric boundary condition as seen in Fig. 10 with 21,600 number of C3D20 three-dimensional quadratic brick elements consisting of 102,052 nodes, which represent bending deformation of the chip well despite high aspect ratio of elements. To calculate the warpage value, we subtract the displacement at the 'B' from the 'A' in the Z direction as shown in Fig. 10.

The FEM results of 100, 80 μm thickness of polyimide/pattern/Si samples and pattern/Si samples (50, 70 and 90 μm) are in a good agreement with test results. However, the FEM simulation result of 50, 60 μm of polyimide/pattern/Si sample deviates from the test results with an error of about 5~30%. To clarify this, we have made a close observation of the profile for all specimens, as illustrated in Fig. 11 (a)~ (d). Fig. 11 shows the warpage shape in terms of the

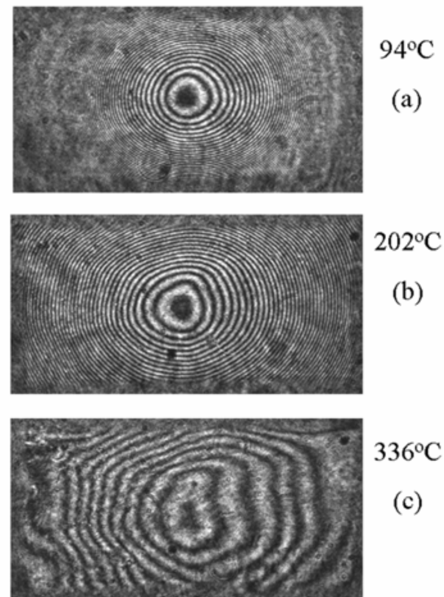

Fig. 8. The profiles of out-of-plane deformation of single chip at various temperatures for polyimide/pattern/Si sample of 100 μm thickness using Twyman-Green interferometer. (0.317 μm per fringe): (a) 94°C (b) 202°C (c) 336°C.

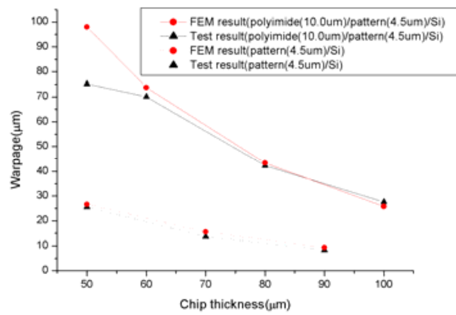

Fig. 9. Comparison of warpage between FEM results and test results.

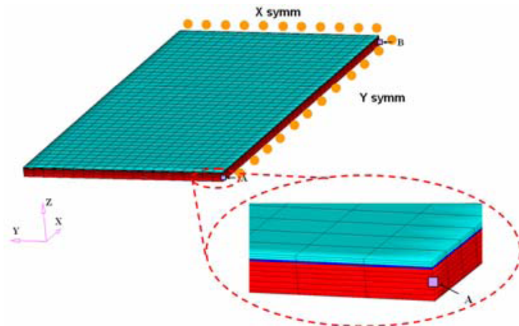

Fig. 10. Finite element meshes of a single chip.

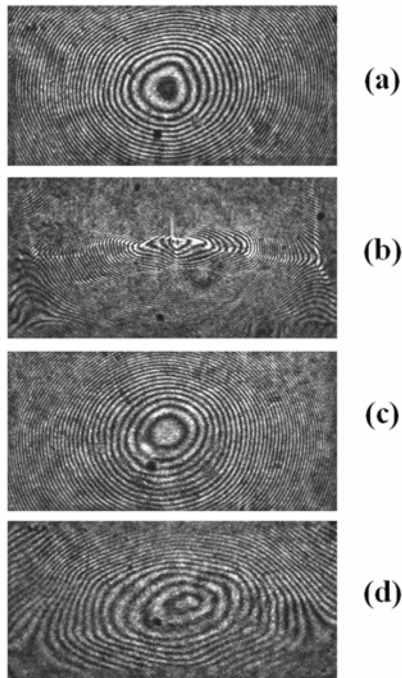

Fig. 11. Warpage profiles of polyimide/pattern/Si samples with the thickness of (a) 100 μm (b) 50 μm ; pattern/Si samples with the thickness of (c) 90 μm (d) 40 μm .

moiré fringe at various thicknesses for both polyimide/pattern/Si and pattern/Si samples. For 50 μm thickness of polyimide/pattern/Si sample, Fig. 11 (b) shows moiré fringe shapes representing irregular and nonuniform wrinkling, while all pattern/Si samples (Fig. 11 (c) and (d)) and 100 μm thick polyimide/pattern/Si sample (Fig. 11 (a)) undergo relatively uniform deflection. The nonuniform wrinkling originates from local instability or buckling occurrence when chip thickness becomes very small. This kind of local nonuniform wrinkling may be well compared with the wrinkling observed in fabrics or clothes. Once this kind of critical state is reached, for accurate evaluation of the deformation profiles we should account for the imperfection of the structure, i.e., the inhomogeneities due to nonuniform bonding between the polyimide layer and the pattern layer, and material properties. However, they may belong to a higher order than considered in first order thermoelastic analysis of the present study, and this is why the present FEM analysis cannot provide a proper prediction of deformations for thin chip structures.

6. Conclusions

In this paper, we have studied the thermomechanical behavior of single chip based on thin silicon substrate with the thickness varying from 100um to 50 um. We have found that the pattern layer plays an important role in the deformation behavior of thin silicon semiconductor chip in contrast to conventional thick chips. We obtained the equivalent material properties of pattern layer by fitting test results to CBA model. For relatively thick chips of 80 and 100 μm , the FEM results are consistent with the experimental results. For the thin chip of 50 μm and 60 μm in thickness, there is about 30% and 5% discrepancy between FEM predictions and the test results, respectively. This has been confirmed, through Twyman-Green interferometer, to be due to the local wrinkling or buckling modes, which is the preferred deformation state or the preferred mode of strain energy relaxation for thin structures.

Acknowledgments

Authors gratefully acknowledge the research support of Device Package Center of Samsung Electronics, and the Korea Science and Engineering Foundation (KOSEF) grant funded by the Korea government (MOST) (R0A-2007-000-20115-0).

References

[1] G. Stoney, The tension of metallic films deposited by electrolysis, *Proc. R. Soc. London A* 82 (1909) 172–175.

[2] E. Suhir, Stresses in bi-metal thermostats, *J. Appl. Mech.* 53 (1986) 657–660.

[3] E. Suhir, Approximate evaluation of the elastic interfacial stresses in the thin films with application to High-T_c superconducting ceramics, *Int. J. Solids Struct. 27* (1991) 1025–1034.

[4] J. S. Kim, K. W. Paik, J. H. Lim and Y. Y. Earmme, Thermomechanical stress analysis of laminated thick-film multilayer substrates, *Appl. Phys. Lett*. 74 (1999) 3507–3509.

[5] J. S. Kim, B. K. Kim, J. H. Lim and K. W. Paik, The finite element analysis of internal stresses during sequential build-up of lamination-based thick-film multilayer substrates, *J. Mat. Sci:Mat. Electr.* 11 (2000) 45–56.

[6] J. S. Kim, S. H. Oh and K. W. Paik, The multilayer-modified Stoney's formula for the laminated polymer composites on a silicon substrate, *J. Appl. Phys.* 86 (1999) 5474–5479.

[7] ABAQUS User's Manual, Hibbit, Karlsson, and Sorenson Inc., Pawtucket, RI (2004).

[8] S. Timoshenko, Analysis of bi-metal thermostats, J. Opt. Soc. Am. 11 (3) (1925) 233.

[9] W. A. Brantley, Calculated elastic constants for stress problems associated with semiconductor devices, *J. Appl*. Phys. 44 (1973) 534–535.

[10] A. S. Voloshin, P. H. Tsao and R. A. Pearson, In situ evaluation of residual stresses in an organic die-attach adhesive, *J. Electron. Packag.* 120 (1998) 314–318.

[11] Y. Guo and S. Liu, Development in optical methods for reliability analysis in electronic packaging applications, *J. Electron. Packag.* 120 (1998) 186–193.